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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/586,909	01/08/2007	Noritaka Muraki	Q79714	1815

23373 7590 07/26/2010
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EXAMINER	
HUBER, ROBERT T	

ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
07/26/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/586,909	MURAKI ET AL.	
	Examiner	Art Unit	
	ROBERT HUBER	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-17 and 19-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-17 and 19-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 May 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's arguments, see page 2 of Remarks, filed May 7, 2010, with respect to claim 1 have been fully considered and are persuasive. The rejection under 35 USC 112, second paragraph of claims 1, 5 – 17 and 19 - 22 has been withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1, 5, 9 – 11, 16, 17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US 6,608,330 B1, prior art of record) in view of Sasaoka

(US 2003/0042496 A1, prior art of record) and Stintz et al. (US 2002/0114367 A1, prior art of record).

a. Regarding claim 1, **Yamada discloses a gallium nitride compound semiconductor light-emitting device** (e.g. figure 1) **comprising**

a crystalline substrate (substrate 101);

a light-emitting layer of a multiple quantum well structure (multiple quantum well structure comprising layers 107 and 108) **that is formed of at least one gallium nitride compound semiconductor barrier layer doped with an impurity element** (layers 107, disclosed in col. 11, lines 7 – 8 to be formed of GaN, InGaN, AlGaN, or the like. E.g. AlGaN may be considered to be doped GaN with impurity element Al) **and at least one gallium nitride compound semiconductor well layer undoped with any impurity element** (layers 108, disclosed in col. 10, lines 3 – 4 to be undoped), **said light-emitting layer being provided on a second side of the crystalline substrate** (e.g. as seen in figure 1);

a contact layer formed of a Group III-V compound semiconductor for providing an Ohmic electrode for supplying device operation current to the light-emitting layer (layer 111, formed from GaN as stated in col. 8, line 41); **and**

an Ohmic electrode (electrode 112)) **that is provided on the contact layer** (e.g. as seen in figure 1) **and has an aperture through which a portion**

of the contact layer is exposed (e.g. as seen in figure 1, the sides of electrode 112 are open, exposing the contact layer 111),

wherein the Ohmic electrode exhibits light permeability with respect to light emitted from the light-emitting layer (col. 10, line 42 discloses the electrode 112 to be transparent), **the individual gallium nitride compound semiconductor well layers of the multiple quantum well structure each has the same composition** (e.g. as seen in figure 1, there are multiple gallium nitride compound semiconductor well layers 108. Since the multiple well layers are all designated as a well layer 108, it is anticipated they are all of the same structure and all have the same composition) **and contains a thick portion having a large thickness** (e.g. col. 13, lines 16 - 36, with reference to figure 6, disclose that the well layers have both thin and thick regions), **and a thin portion having a thickness 1.5 nm or less** (col. 13, lines 20 – 22 disclose that, with reference to figure 6, disclose that the well layers have regions with thickness less than half of the average thickness. Col. 9, lines 35 - 36 discloses the average thickness of a well layer to be 3 nm. Therefore, the regions defined by "D" in figure 6 of the well layers are less than 1.5 nm)**;**

wherein the at least one gallium nitride compound semiconductor well layer is a discontinuous layer (A common definition of “discontinuous" is "marked by breaks or interruptions". col. 13, lines 20 – 22 disclose that, with reference to figure 6, the well layer may be considered as having “breaks" or

“interruptions” in regions with lower thicknesses than other regions, and there for the well layer may be considered as "discontinuous").

Yamada is silent with respect to explicitly disclosing the at least one gallium nitride compound semiconductor well layer includes a portion having zero thickness, such that the at least one gallium nitride compound semiconductor layer is absent a portion (see 112 2nd rejection above). However, Yamada does disclose the at least one gallium nitride compound semiconductor layer may have a thickness of “less than a half of an average thickness” of the layer (page 13, lines 20 - 23).

Stintz discloses that a gallium compound semiconductor well layer of a light emitting device may have a portion having zero thickness, such that the at least one gallium nitride compound semiconductor layer is absent a portion (as seen in figure 11C, layer 408 has portions that are zero thickness, such that layers 406 exists between the layer 408).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Yamada such that the at least one gallium nitride compound semiconductor well layer includes a portion having zero thickness, such that the at least one gallium nitride compound semiconductor layer is absent a portion, since Yamada discloses the layer to have portions with a thickness of less than half the average thickness of the layer, and a zero thickness is less than half the average thickness. And, it has been held that in the case where the claimed ranges overlap or lie inside the

ranges disclosed by the prior art, then a prima facie case of obviousness exists (See MPEP 2144.05). Furthermore, Stintz discloses that quantum well layers may be discontinuous such that there are regions of the layer with zero thickness. One would have been motivated to have a portions of the well layer with zero thickness in order to create quantum confinement regions that would alter the characteristics of the light emitting layer, allowing one to control and optimize the light emitted by the device (as seen in figure 12 of Stintz).

Yamada is also silent with respect to disclosing the barrier layer is doped with a Group IV element at an average atom density of 1 x 10^{17} cm^{-3} to 5 x 10^{18} cm^{-3}.

Sasaoka discloses a gallium nitride compound semiconductor light-emitting device with barrier layer being doped with a Group IV element at an average atom density of $1x10^{17}$ cm^{-3} to $5x10^{18}cm^{-3}$ which exhibits a low resistance (¶ [0109] discloses the barrier layer to be Si doped with a concentration of $1x10^{18}$ cm^{-3}).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Yamada such that the barrier layers are doped with a Group IV compound with a density of $1x10^{17}$ cm^{-3} to $5x10^{18}cm^{-3}$ since it was known that gallium nitride compound light emitting devices can contain quantum well layers comprising barrier layers with such dopant and concentrations, as disclosed by Sasaoka. One would have been motivated to make the barrier layer with a dopant of Group IV materials since these would

create an n-type semiconductor barrier layer, allowing one to control the conductivity of the barrier layer, resulting in a more efficient light emission properties of the quantum well.

Regarding the limitation of doping the barrier layer "*for the purpose of decreasing forward voltage of the device*", this is regarded as a statement of intended use, and it has been held by the courts that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham 2 USPQ2d 1647 (1987). See MPEP 2114.

b. Regarding claim 5, **Yamada in view of Sasaoka and Stintz further disclose a gallium nitride compound semiconductor light-emitting device, as cited above, wherein the predetermined impurity element added only to the barrier layer is silicon** (Yamada: col. 10, lines 3 – 7, disclose that the layer 108 may be doped with Silicon. Col. 9, line 62 discloses the layer 108 may be a barrier layer).

c. Regarding claim 9, **Yamada in view of Sasaoka and Stintz disclose a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above, however Yamada is silent with respect to the**

contact layer having a thickness of 1 μm to 3 μm, however Yamada discloses that the contact layer thickness is 0.25 μm.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to enlarge the layer thickness of Yamada in view of Sasaoka, since it has been held by the courts that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device, and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device. *In Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984). One would be motivated to make such a modification of the layer thickness in order to make the device structurally more rigid.

d. Regarding claim 10, **Yamada in view of Sasaoka and Stintz disclose a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above, wherein the Ohmic electrode (18) exhibits a transmittance at the wavelength of emitted light of 30% or higher** (the structure of Yamada in view of Sasaoka are obvious over the structure of the claimed invention, therefore Yamada in view of Sasaoka are obvious over the properties of the light transmittance of the Ohmic electrode, since it has been held that when the prior art discloses the structure of the claimed invention, a

prima facie case of anticipation or obviousness of the inherent properties has been established. See MPEP 2112.01.)

e. Regarding claim 11, **Yamada in view of Sasaoka and Stintz further disclose a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above, wherein the Ohmic electrode has a thickness of 1 nm to 100 nm** (Yamada: col. 10, lines 42 – 43, disclose the electrode has a thickness of 20 nm).

f. Regarding claims 16 and 17, **Yamada in view of Sasaoka and Stintz further disclose a lamp and an LED employing the gallium nitride compound semiconductor light- emitting device according to claim 1** (Yamada: col. 11, lines 25 – 36).

g. Regarding claim 19, **Yamada in view of Sasaoka and Stintz further disclose a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above, wherein the at least one barrier layer is an Si-doped n-type GaN barrier layer** (Sasaoka: ¶ [0109] discloses the Group IV doped GaN barrier layer to be Si doped n-type GaN).

5. Claims 6 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view Sasaoka and Stintz, as cited above with respect to claim 1, and in further view of Hanaoka et al. (US 5,804,839, prior art of record).

a. Regarding claim 6, **Yamada in view of Sasaoka and Stintz disclose a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above. However, Yamada, Sasaoka, and Stintz are silent with respect to the contact layer being doped with an n- type impurity element and has a carrier concentration of 5 x 10^{18} cm^{-3} to 2 x 10^{19} cm^{-3}.**

Hanaoka teaches that GaN layers may be formed with n-type impurity concentrations of 1 x 10^{19} cm^{-3} (col. 9, lines 20 - 23).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the contact layer of Yamada in view Sasaoka and Stintz to include n-type impurities with a concentration of 1 x 10^{19} cm^{-3} since Hanaoka discloses that this is known structure used for light emitting devices. One would have been motivated to make such a modification since it would allow the layer to exhibit light transmission properties, allowing the light to transmit readily through the layer, and desirable electrical properties for tuning the light emitting device.

b. Regarding claims 7 and 8, **Yamada in view of Sasaoka and Stintz disclose a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above, wherein the contact layer is doped**

with a p - type impurity element (Yamada: col. 8, line 41). **Yamada, Sasaoka, and Stintz are silent with respect to the layer having a carrier concentration of 1 x 10^{17} cm^{-3} to 1 x 10^{18} cm^{-3}.**

Hanaoka teaches that p-type contact layers may be doped with a carrier concentration of 1 x 10^{18} cm^{-3} (col. 3, lines 48 – 49).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the contact layer of Yamada in view of Sasaoka and Stintz to have a p-type impurity concentration of 1 x 10^{18} cm^{-3} since Hanaoka discloses that this is known contact layer structure used in light emitting devices. One would have been motivated to make such a modification since it would allow the layer to exhibit light transmission properties, allowing the light to transmit readily through the layer, and desirable electrical properties for tuning the light emitting device.

6. Claims 12, 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Sasaoka and Stintz, as applied to claim 1 above, and in further view of Morita et al. (US 6,121,636, prior art of record). **Yamada in view of Sasaoka and Stintz disclose a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above, however Yamada, Sasaoka, and Stintz are silent with respect to a multilayered metallic reflecting mirror made of the same material identical to the Ohmic electrode for reflecting light emitted**

from the light-emitting layer to the outside, which is provided on a first side of the crystalline substrate.

Morita discloses a mirror on the outside first side of the crystalline substrate (e.g. figure 1, reflecting layer 11) **wherein the metallic reflecting mirror contains a metallic material identical to that contained in the Ohmic electrode** (e.g. col. 4, lines 1 – 9, discloses that the layer may be made of gold, which is the same material as the electrode 9). **Morita further discloses that the layers may be multilayered** (col. 2, lines 21 - 25).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the light emitting device of Yamada in view of Sasaoka and Stintz to include the reflecting mirror, as taught by Morita, since Morita discloses that multilayer reflecting mirrors, made of the same material as the electrode, can be added to light emitting devices. One would be motivated to add a reflecting mirror on the second side of the substrate in order to prevent light escaping from the bottom of the device, thereby protecting underlying structures, as taught in Morita in col. 8, lines 33 - 44. One would be motivated to make the reflecting mirror multilayered to enhance it reflecting ability. One would further be motivated to make the mirror of the same material as that of the Ohmic electrode since it would require fewer materials for the production process.

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Sasaoka and Stintz, as applied to claim 1 above, and in further view of

Kaneyama et al. (US 6,452,214 B2, prior art of record). **Yamada in view of Sasaoka and Stintz disclose a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above, however Yamada, Sasaoka, and Stintz are silent with respect to a metallic reflecting mirror containing a single-metal film or an alloy film formed from at least one member selected from the group consisting of silver, platinum, rhodium and aluminum.**

Kaneyama teaches a metallic reflecting mirror formed from aluminum (col. 4, lines 32 - 35).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the light emitting device of Yamada in view of Sasaoka and Stintz to include the reflecting mirror, as taught by Kaneyama, since Kaneyama discloses that reflecting mirrors made of aluminum can be added to light emitting devices. One would be motivated to add an aluminum reflecting mirror on the second side of the substrate in order to prevent light escaping from the bottom of the device, thereby protecting underlying structures, and aluminum is a readily available material that is can be relatively easily deposited on substrates via known deposition methods (i.e. sputtering, evaporation, etc...)

8. Claims 20 – 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Sasaoka and Stintz as applied to claim 1 above, and further in view of Lester (US 6,291,839 B1, prior art of record).

a. Regarding claim 20, **Yamada in view of Sasaoka and Stintz disclose a gallium nitride compound semiconductor light-emitting device according to claim 1, but are silent with respect to apertures are formed such that a total surface area of the apertures accounts for 30% to 80% of a surface of the contact layer.**

Lester discloses a gallium nitride compound semiconductor light-emitting device (e.g. figure 1), **wherein apertures are formed in an Ohmic electrode** (openings in p-type contact 20, as disclosed in col. 3, lines 1 - 3) **such that a total surface area of the apertures accounts for 30% to 80% of a surface of the contact layer** (as disclosed in col. 4, lines 34 - 35).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the gallium nitride semiconductor light-emitting device of Yamada in view of Sasaoka and Stintz such that the Ohmic electrode comprises a apertures with a total surface area of 30 - 80% of the surface of contact layer since Lester discloses a similar device with similar structure wherein apertures with such configurations may be formed. One would have been motivated to have apertures of such dimensions in order to optimize light transmittance from the device while providing an even Ohmic contact, as discussed by Lester (col. 3, lines 34 - 40).

b. Regarding claim 21, **Yamada in view of Sasaoka and Stintz disclose gallium nitride compound semiconductor light-emitting device according to**

claim 1, wherein a metallic film consists the Ohmic electrode (Yamada: col. 10, lines 42 – 43 disclose electrode 112 to be gold and nickel). **Yamada in view of Sasaoka and Stintz are silent with respect to a minimum horizontal width (lateral width) of the metallic film consisting the Ohmic electrode is 10 μm or less, and a horizontal width of the aperture is 0.5 μm to 50 μm.**

Lester discloses a gallium nitride compound semiconductor light-emitting device (e.g. figure 1), **wherein a horizontal width of the aperture is 0.5 μm to 50 μm** (e.g. figure 1 and col. 3, lines 1 -3 disclose that the Ohmic layer may comprise openings (apertures). Col. 3, lines 21 – 22 disclose the dimensions of the openings). **Lester also discloses that a total surface area of the apertures accounts for 30% to 80% of a surface of the contact layer** (as disclosed in col. 4, lines 34 - 35).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Yamada in view of Sasaoka and Stintz such that the Ohmic electrode comprises apertures with a horizontal width of 0.5 μm to 50 μm since Lester discloses a similar device with an Ohmic layer comprising apertures of such dimensions. One would have been motivated to have the apertures of a width between 0.5 μm to 50 μm in order to maximize current flow in the Ohmic contact while optimizing the light transmittance through the apertures of the Ohmic layer, as discussed by Lester (col. 3, lines 5 – 22).

The combination of Yamada in view of Sasaoka and Stintz with the teachings of Lester disclose a device that is obvious over the limitation of a

minimum horizontal width (lateral width) of a metallic film consisting the Ohmic electrode is 10 μm or less. Yamada discloses the device to have an area of 350 μm square (col. 10, line 53), **of which the Ohmic layer of Yamada in view of Sasaoka and Lester comprises a large portion** (e.g. as seen in figures 1 of Yamada and Lester). **Since Lester discloses the total surface area of the apertures to account for 20 - 80% of the surface area, and the dimensions of the apertures to be 0.5 – 20 μm, one may do the calculations to find the average horizontal distance between the apertures to be about 0.4 μm.**

Although this calculation is done using an estimated contact layer size similar to the size of the area of device as disclosed by Yamada, and average homogeneous distribution of apertures within the Ohmic contact layer, a prima facie case of obviousness is established that a minimum horizontal width of the metallic film comprising the Ohmic electrode is 10 μm or less, and it has been held that when the prior art discloses the general conditions of the claimed invention, discovering the optimum or workable ranges involves only ordinary skill in the art. See MPEP 2144.05. One would have been motivated to have a minimum horizontal distance of the metallic film comprising the Ohmic electrode of 10 μm or less in order to optimize the current flow in the Ohmic contact while optimizing the light transmittance through the apertures of the Ohmic layer, as discussed by Lester (col. 3, lines 5 – 22).

c. Regarding claim 22, **Yamada in view of Sasaoka and Stintz and in further view of Lester disclose a gallium nitride compound semiconductor light-emitting device according to claim 20, wherein a horizontal width of the aperture is 0.5 mm to 50 mm** (Lester: col. 3, line 22).

Regarding the claim limitation "wherein a minimum horizontal width (lateral width) of a metallic film consisting the Ohmic electrode is 10 mm or less", the combination of Yamada in view of Sasaoka and Stintz with the teachings of Lester disclose a device that is obvious over the limitation of a minimum horizontal width (lateral width) of a metallic film comprising the Ohmic electrode is 10 μm or less. Yamada discloses the device to have an area of 350 μm square (col. 10, line 53), **of which the Ohmic layer of Yamada in view of Sasaoka and Lester comprises a large portion** (e.g. as seen in figures 1 of Yamada and Lester). **Since Lester discloses the total surface area of the apertures to account for 20 - 80% of the surface area, and the dimensions of the apertures to be 0.5 – 20 μm, one may do the calculations to find the average horizontal distance between the apertures to be about 0.4 μm.**

Although this calculation is done using an estimated contact layer size similar to the size of the area of device as disclosed by Yamada, and average homogeneous distribution of apertures within the Ohmic contact layer, a prima facie case of obviousness is established that a minimum horizontal width of the metallic film comprising the Ohmic electrode is 10 μm or less, and it has been

held that when the prior art discloses the general conditions of the claimed invention, discovering the optimum or workable ranges involves only ordinary skill in the art. See MPEP 2144.05. One would have been motivated to have a minimum horizontal distance of the metallic film comprising the Ohmic electrode of 10 μm or less in order to optimize the current flow in the Ohmic contact while optimizing the light transmittance through the apertures of the Ohmic layer, as discussed by Lester (col. 3, lines 5 – 22).

Response to Arguments

9. Applicant's arguments with respect to the rejection of claims under 35 USC 103, filed May 7, 2010, have been fully considered but they are not persuasive.

a. The Applicant argues that the Examiner's interpretation of *the "multiple quantum well structure*" to comprise only layers 107 and 108 of the device of figure 1 of Yamada is incorrect, and that layer 109 should also be included within the "*multiple quantum well structure*" (see pgs. 5 – 6 of Remarks). The Examiner respectfully disagrees, and maintains the argument presented in the prior office action with respect to the interpretation of the "*multiple quantum well structure*" (see Response to Arguments, ¶ 10, in office action filed January 7, 2010). The Examiner reiterates that the term "*structure*" is a term of broad meaning, since the definition of "*structure*" is "*something that is constructed*" (Merriam-Webster's Collegiate Dictionary, 10th Edition, 2001). One may indeed interpret the device of Yamada as seen in figure 1 in several different ways, including the quantum well

structure to comprise several multiple quantum well structures, with one structure comprising layers 107 and 108, and a second structure comprising layers 109 and layer 108 above layer 109, as the Examiner has done in the rejection cited above. In the Applicant's remarks, the Applicant has interpreted the multiple quantum well structure to comprise all layers 107, 108, and 109. Although the Examiner acknowledges this interpretation may be valid, it is not a limiting interpretation since the claims are to be given their broadest reasonable interpretation, and the term "*structure*" is a term of broad scope and leads to several different interpretations of the multiple layer quantum well structure. The Examiner maintains that the interpretation presented in the rejection above is also valid, and hence the rejection is maintained.

Furthermore, with respect to the Applicant's argument that the Examiner is modifying the device of Yamada due to the interpretation of the "*multiple quantum well structure*" to comprise layers 107 and 108 (see bottom of pg. 6 of Remarks), the Examiner respectfully disagrees. The Examiner is not modifying the "*multiple quantum well structure*" of Yamada with respect to the interpretation, but only broadly interpreting what is meant by "*multiple quantum well structure*". Such in interpretation does not preclude additional multiple quantum well structures, such as that including layers 109 and 108 on top of 109, as seen in figure 1 of Yamada.

b. The Applicant argues that the prior art of Stintz does not disclose or render obvious the limitation of "*the at least one gallium nitride compound semiconductor well layer is a discontinuous layer including a portion having a thickness of 0 nm*" (see pgs 7 - 8 of Remarks). The Applicant argues that Stintz does not disclose a portion of the total thickness of the quantum well layer to be 0 nm (see top of pg 8 of Remarks), and therefore will not render obvious the claimed limitation when combined with the prior art of Yamada. The Examiner respectfully disagrees. The Examiner notes that the Applicant is interpreting the quantum well layer structure in a different manner than what the Examiner has interpreted, and therefore states that multiple layers of the quantum well structure do not have a discontinuous thickness, and nowhere is a portion zero thickness. It is common in the art that layers may comprise sub-layers, and that a sub-layer may also be referred to as a layer. Stintz clearly shows in figure 11c that the quantum well layer 408 is discontinuous and has portions of zero thickness. The Examiner has not substituted the entire quantum well structure of Stintz into the quantum well structure of Yamada, but rather has used Stintz as a supporting reference to show that it is indeed advantageous to have a discontinuous well layer (sublayer) within the quantum well structure. As cited above with respect to claim 1, Yamada teaches that, indeed, that portions of the layers within the quantum well structure have varying thicknesses, as seen in figure 6, and Stintz is used as a supporting reference to teach the layers may actually have portions of zero thickness. Furthermore, optimization and device processing of the layers

of Yamada may also yield portions of zero thickness. Therefore, the Examiner maintains that Yamada in view of Stintz renders obvious the limitation of the well layer being discontinuous and having a portion of zero thickness.

With regards to the Applicants arguments with respect to layer 406 and protruding portions 1105 (see pg. 8 of Remarks), the Examiner does not rely on these layers for support of the claimed invention, but rather on the discontinuous well layer 408. Therefore, the arguments are not persuasive.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is

(571)270-3899. The examiner can normally be reached on Monday - Friday (11am - 7pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thao X Le/
Supervisory Patent Examiner, Art Unit 2892

/Robert Huber/
Examiner, Art Unit 2892
July 19, 2010